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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/757,123	01/09/2001	Satish Athavale	01P7408US	6586

7590 10/23/2002

Siemens Corporation
Intellectual Property Department
186 Wood Avenue South
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EXAMINER
BROWN, CHARLOTTE A

ART UNIT	PAPER NUMBER
1765	10

DATE MAILED: 10/23/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

AS-10

Office Action Summary

Application No.	Applicant(s)
09/757,123	Athavale et al.
Examiner	**Art Unit**
Charlotte Brown	1765

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) ☒ Responsive to communication(s) filed on *Oct 3, 2002*

2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.

3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

Disposition of Claims

4) ☒ Claim(s) *1-31* is/are pending in the application.

4a) Of the above, claim(s) _____ is/are withdrawn from consideration.

5) ☐ Claim(s) _____ is/are allowed.

6) ☒ Claim(s) *1-31* is/are rejected.

7) ☐ Claim(s) _____ is/are objected to.

8) ☐ Claims _____ are subject to restriction and/or election requirement.

Application Papers

9) ☐ The specification is objected to by the Examiner.

10) ☐ The drawing(s) filed on _____ is/are a) ☐ accepted or b) ☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13) ☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a) ☐ All b) ☐ Some* c) ☐ None of:

1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

*See the attached detailed Office action for a list of the certified copies not received.

14) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

a) ☐ The translation of the foreign language provisional application has been received.

15) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s). _____
4) ☐ Interview Summary (PTO-413) Paper No(s). _____
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claim 1-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Singh et al. (US 6,042,687) in view of DeOrnellas et al. (US 6,046,116) and further in view of Yang (US 5,827,437) and Muller et al. (US 5,605,600).

Singh discloses a plasma processing system and method for processing substrates. The plasma processing system comprises a processing chamber enclosing a substrate support assembly. The substrate support may comprise an RF powered electrode (Column 3, lines 60-67). The substrate may be clamped to the electrode (Column 4, lines 3-4). A substrate is processed in the processing chamber by energizing a process gas into a high density plasma. This reads on the applicant's limitation of a wafer comprising a silicon substrate.

Unlike the claimed invention, Singh does not teach a method for heating the wafer to temperature greater than 200 degrees Celsius.

DeOrnellas discloses a method for performing an etch operation in a reactor. A wafer is positioned over a bottom electrode in an etching chamber (Column 3, lines 6-9). A wafer clamp

holds the wafer against a lower electrode (Column 3, lines 36-40). A resistance heater is contained in the lower electrode. The electrode is heated in order to heat the wafer (Column 3, lines 49-55). During etching, the temperature of the wafer reaches 275^{0}C (Column 4, lines 38-40). The Helium pressure is generally about 3 torr or greater (Column 4, lines 6-10). This reads on the applicant's limitation of applying a backside pressure of about 6 torr or greater.

It is the Examiner's position that a person having ordinary skill in the art would have found it obvious to modify Singh with the method of heating the wafer to a temperature of greater than 200^{0}C as taught by DeOrnellas. This additional step would have been anticipated in order to control the temperature of the wafer which would minimize the critical dimension growth (DeOrnellas, Column 1, lines 55-57).

Unlike the claimed invention, neither Singh nor DeOrnellas teaches a method for exposing the wafer to a reactive plasma to etch trenches into the wafer.

Yang discloses a plasma reactor. A wafer is introduced into the chamber and disposed on an electrostatic chuck which acts as an electrode an is biased by an RF generator. The wafer is clamped onto an electrostatic chuck. A helium cooling gas may be introduced under pressure to act as a heat transfer medium for accurately controlling the wafer's temperature during processing to ensure uniform etching results (Column 5, lines 23-40). A plasma is created from an etchant source gas in order to etch a wafer (Column 5, lines 45-47). The gas includes Cl_2, BCl_3, and N_2 or Ar. An antireflective coating layer, a hardmask layer, is formed over the silicon substrate. This reads on the applicant's limitation of forming a hardmask on a silicon substrate of

a wafer. A patterned photoresist layer is formed over the hardmask layer (Column 10, lines 55-60). The etchant source gas is used to etch narrow trenches into the wafer (See Figure 1B).

It is the Examiner's position that a person having ordinary skill in the art would have found it obvious to modify Singh and DeOrnellas with the method of exposing the wafer to a plasma to etch trenches in the wafer as taught by Yang since Singh is not particular about the type of structures formed as a result of plasma etching. Therefore, the formation of trenches would have been anticipated in order to achieve a reasonable expectation of success.

Unlike the claimed invention, neither Singh, DeOrnellas, nor Yang teach a method for etching deep trenches in a substrate that have an etching depth of about 7*u*m or greater.

Muller teaches a method of etch profile shaping through wafer temperature control. A deep trench etch which produces a desired trench profile is performed using a hardmask including layers of different materials. Within the first minute, an etch depth of approximately 1.5 *u*m is reached. The remaining six minutes of the etching period create approximately 6 *u*m of additional etching depth. This reads on the applicant's limitation of etching deep trenches into a silicon substrate of the wafer in accordance with the hardmask pattern wherein the deep trenches have a depth of about 7 *u*m or greater.

It is the Examiner's position that a person having ordinary skill in the art would have found it obvious to modify Singh, DeOrnellas, and Yang with the method of etching deep trenches into the substrate as taught by Muller. The additional step of forming deep trenches in

the substrate would have been anticipated in order to produce a tapered trench sidewall which is the optimum trench profile (Column 3, lines 13-25).

3. Claims 16-31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Singh et al (US 6,042,687) in view of DeOrnellas et al. (US 6,046,116) and further in view of Yang (US 5,827,437) and Muller et al. (US 5,605,600).

Singh discloses a plasma processing system and method for processing substrates. The plasma processing system comprises a processing chamber enclosing a substrate support assembly. The substrate support may comprise an RF powered electrode (Column 3, lines 60-67). The substrate may be clamped to the electrode (Column 4, lines 3-4). A substrate is processed in the processing chamber by energizing a process gas in the processing chamber into a high density plasma. The process gas can include a mixture of Cl_2 and BCl_3. A secondary gas supply can comprise one or more inert gases such as argon or helium and a substrate passivating gas such as nitrogen or oxygen. Therefore, the wafer is exposed to a reactive plasma including Cl_2, BCl_3, Ar, O_2, and N_2 (Column 4, lines 29-46). The substrate is cooled through backside helium cooling. In one example, 8 Torr of backside helium pressure is applied (Column 6, lines 9-14). The baseline parameters are 150 sccm of Cl_2 , 10 mTorr of chamber pressure, 200 Watts of bias power supplied to the substrate holder, 6 Torr of He backside pressure, and 60^0C for the chamber and electrode temperatures. The wafer is clamped to the electrode (Column 4, lines 3-4). Therefore,

the heat from the electrode is transferred to the wafer. This reads on the applicant's limitation of maintaining the wafer at about the same temperature as the electrode.

Unlike the claimed invention, Singh does not teach a method for heating the wafer to temperature greater than 200 degrees Celsius.

DeOrnellas discloses a method for performing an etch operation in a reactor. A wafer is positioned over a bottom electrode in an etching chamber (Column 3, lines 6-9). A wafer clamp holds the wafer against a lower electrode (Column 3, lines 36-40). A resistance heater is contained in the lower electrode. The electrode is heated in order to heat the wafer (Column 3, lines 49-55). During etching, the temperature of the wafer reaches 275^{0}C (Column 4, lines 38-40). The helium pressure is generally about 3 torr or greater (Column 4, lines 6-10). This reads on the applicant's limitation of applying a backside pressure of about 6 torr or greater.

It is the Examiner's position that a person having ordinary skill in the art would have found it obvious to modify Singh with the method of heating the wafer to a temperature of greater than 200^{0}C as taught by DeOrnellas. This additional step would have been anticipated in order to control the temperature of the wafer which would minimize the critical dimension growth.

Unlike the claimed invention, neither Singh nor DeOrnellas teaches a method for exposing the wafer to a reactive plasma to etch trenches into the wafer.

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Muller teaches a method of etch profile shaping through wafer temperature control. A deep trench etch which produces a desired trench profile is performed using a hardmask including layers of different materials. Within the first minute, an etch depth of approximately 1.5 *u*m is reached. The remaining six minutes of the etching period create approximately 6 *u*m of additional etching depth. This reads on the applicant's limitation of etching deep trenches into a

silicon substrate of the wafer in accordance with the hardmask pattern wherein the deep trenches have a depth of about 7 *u*m or greater.

It is the Examiner's position that a person having ordinary skill in the art would have found it obvious to modify Singh, DeOrnellas, and Yang with the method of etching deep trenches into the substrate as taught by Muller. The additional step of forming deep trenches in the substrate would have been anticipated in order to produce a tapered trench sidewall which is the optimum trench profile (Column 3, lines 13-25).

4. Any inquiry concerning this communications from the Examiner should be directed to Charlotte A. Brown whose telephone number is (703) 305-0727. The Examiner can normally be reached during the hours of 9:00AM to 6:30PM.

The fax phone numbers for the organization where this application or proceeding is assigned are 703-872-9310 for regular communications and 703-872-9311 for After Final communications.

CAB

October 18, 2002

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